List of publications of Dragomir Milojevic

List fulfilling the Guide for applicants 2018's requirements

1. Published works, as an author, a co-author or a publisher

1. **Milojevic, D.** (2018). *Handbook of 3D Integration: Ultra-Fine Pitch 3D-Stacked Integrated Circuits: Technology, Design*.

2. Doan, N. A. V., **Milojevic, D.**, & De Smet, Y. (2017). *MCDM Applied to the Partitioning Problem of 3D-Stacked Integrated Circuits*. Springer International Publishing, Springer.

3. Gogniat, G., **Milojevic, D.**, Morawiec, A., & Erdogan, A. (2010). *Algorithm-Architecture Matching for Signal and Image Processing: Best Papers from Design and Architectures for Signal and Image Processing 2007 & 2008 & 2009*. Springer.

4. Rupp, M., **Milojevic, D.**, & Gogniat, G. (2008). *Design and Architectures for Signal and Image Processing*. Hindawi Publishing Corporation.

5. Viviers, D., **Milojevic, D.**, & Warzée, N. (2005). *3D Reconstruction of the Necropolis in Itanos, Crete: Proceedings of the 10th International Conference « Cultural Heritage and New Technologies*. Vienne.

2. Book chapters or participation to a collective book, as an author or a co-author of the section

1. **Milojevic, D.**, Varadarajan, R., Seynhaeve, D., & Marchal, P. (2011). Path finding and techtuning. In *Three Dimensional System Integration: IC Stacking Process and Design* (pp. 137-185). Springer US. doi:10.1007/978-1-4419-0962-6_7

2. **Milojevic, D.**, Varadarajan, R., Seynhaeve, D., & Marchal, P. (2010). PathFinding and TechTuning. In A. Papanikolaou, D. Soudris, & R. Radojcic (Eds.), *hree Dimensional System Integration: IC Stacking Process and Design* (pp. 137-186). Springer.

3. **Milojevic, D.**, Martin, P., Leroy, A., Robert, F., & Verkest, D. D. (2009). NoC based implementation: MPSoC for high-performance, low-power video coding application. In *Networks-on-chips: Theory and practice*. Faye Publisher, Taylor and Francis Group LLC, CRC Press.

3. Articles published in peer-review journals

1. Luca, M., **Milojevic, D.**, & Debacker, P. (2018). Post Place and Route Design-Technology Co-Optimization for scaling at single digit nodes with constant ground rules. *Journal of Micro/Nanolithography, M E M S, and M O E M S*,(1932-5150).

2. Rethinagiri, S. K., Palomar, O., Sobe, A., Yalcin, G., Knauth, T., Gil, R. T., Prieto, P., Schneegass, M., Cristal, A., Unsal, O., Felber, P., Fetzer, C., & **Milojevic, D.** (2015).

ParaDIME: Parallel Distributed Infrastructure for Minimization of Energy for data centers. *Microprocessors and microsystems*, 191-198. doi:10.1016/j.micpro.2015.06.005

3. Maggioni, F. L. T., Oprins, H., **Milojevic, D.**, Beyne, E., Wolf, I. D., & Baelmans, M. (2015). 3D-convolution based fast transient thermal model for 3D integrated circuits: Methodology and applications. *Annual IEEE Semiconductor Thermal Measurement and Management Symposium*,, 7100148 107-112. doi:10.1109/SEMI-THERM.2015.7100148

4. Agrawal, P., **Milojevic, D.**, Raghavan, P., Catthoor, F., Van der Perre, L., Beyne, E., & Varadarajan, R. (2014). System Level Comparison of 3D Integration Technologies for Future Mobile MPSoC Platform. *I E E E Embedded Systems Letters*, *6*(4), 85-88. doi:10.1109/LES.2014.2360642

5. Doan, N. A. V., **Milojevic, D.**, Robert, F., & De Smet, Y. (2014). A MOO-based methodology for designing 3D-stacked integrated circuits. *Journal of multi-criteria decision analysis*, *21*(1-2), 43-63. doi:10.1002/mcda.1497
https://dipot.ulb.ac.be/dspace/bitstream/2013/134817/3/134817.pdf

6. Allard, Y., Nelissen, G., Goossens, J., & **Milojevic, D.** (2014). A Context Aware Cache Controller to Bridge the Gap Between Theory and Practice in Real-Time Systems. *Proceedings (International Conference on Real-Time Computing Systems and Applications)*. doi:http://dx.doi.org/10.1109/RTCSA.2014.6910503
https://dipot.ulb.ac.be/dspace/bitstream/2013/163473/1/rtcsa2014_submission_140.pdf

7. Nelissen, G., Berten, V., Nélis, V., Goossens, J., & **Milojevic, D.** (2012). U-EDF: An Unfair but Optimal Multiprocessor Scheduling Algorithm for Sporadic Tasks. *Proceedings (Euromicro Conference on Real-Time Systems)*, 13-23. doi:http://dx.doi.org/10.1109/ECRTS.2012.36
https://dipot.ulb.ac.be/dspace/bitstream/2013/151588/1/U-EDF-ECRTS2012.pdf

8. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2012). Techniques Optimizing the Number of Processors to Schedule Multi-Threaded Tasks. *Proceedings (Euromicro Conference on Real-Time Systems)*, 321-330. doi:http://dx.doi.org/10.1109/ECRTS.2012.37
https://dipot.ulb.ac.be/dspace/bitstream/2013/151590/1/Multithread-ECRTS2012.pdf

9. Nelissen, G., Funk, S., Goossens, J., & **Milojevic, D.** (2011). Swapping to Reduce Preemptions and Migrations in EKG. *SIGBED review*, *8*(3), 36-39.

10. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2011). Reducing Preemptions and Migrations in Real-Time Multiprocessor Scheduling Algorithms by Releasing the Fairness. RTCSA. *Proceedings (International Conference on Real-Time Computing Systems and Applications)*.

11. Airoldi, R. R., Ahonen, T. T., Garzia, F. F., **Milojevic, D.**, & Nurmi, J. J. (2011). Implementation of W-CDMA Cell Search on a Highly Parallel and Scalable MPSoC. *Journal of Signal Processing Systems*.

12. Garzia, F. F., Airoldi, R. R., Ahonen, T. T., Nurmi, J. J., & **Milojevic, D.** (2009). Implementation of the W-CDMA cell search on a MPSOC designed for software

defined radios. *IEEE Workshop on Signal Processing Systems, SiPS: Design and Implementation*,, 5336244 30-35. doi:10.1109/SIPS.2009.5336244

13. Airoldi, R. R., Garzia, F. F., Ahonen, T. T., **Milojevic, D.**, & Nurmi, J. J. (2009). Implementation of W-CDMA cell search on a FPGA based multi-processor system-on-chip with power management. *Lecture notes in computer science*, *5657 LNCS*, 88-97. doi:10.1007/978-3-642-03138-0_10

14. **Milojevic, D.**, Montperrus, L. L., & Verkest, D. D. (2009). Power dissipation of the network-on-chip in multi-processor system-on-chip dedicated for video coding applications. *Journal of Signal Processing Systems*, *57*(2), 139-153. doi:10.1007/s11265-008-0251-1

15. Goossens, J., **Milojevic, D.**, & Nélis, V. (2008). Power-aware real-time scheduling upon dual CPU type multiprocessor platforms. *Lecture notes in computer science*, *5401 LNCS*, 388-407. doi:10.1007/978-3-540-92221-6_25
https://dipot.ulb.ac.be/dspace/bitstream/2013/69291/1/69291.pdf

16. Leroy, A., **Milojevic, D.**, Verkest, D. D., Robert, F., & Catthoor, F. (2008). Concepts and implementation of spatial division multiplexing for guaranteed throughput in networks-on-chip. *I.E.E.E. transactions on computers*, *57*(9), 1182-1195. doi:10.1109/TC.2008.82

17. Vander Biest, A., Richard, A., **Milojevic, D.**, & Robert, F. (2008). A multi-objective and hierarchical exploration tool for SoC performance estimation. *Lecture notes in computer science*, *5114 LNCS*, 85-95. doi:10.1007/978-3-540-70550-5_10

18. Rupp, M., **Milojevic, D.**, & Gogniat, G. (2008). Design and architectures for signal and image processing. *EURASIP Journal on Embedded Systems*, *2008*(1), 275975. doi:10.1155/2008/275975

19. Nélis, V., Goossens, J., Navet, N., Devillers, R., & **Milojevic, D.** (2008). Power-Aware Real-Time Scheduling upon Identical Multiprocessor Platforms. *Proceedings of the IEEE International Conference on Sensor Network, Ubiquitous, and Trustworthy Computing*, 209-216. doi:http://dx.doi.org/10.1109/SUTC.2008.31
https://dipot.ulb.ac.be/dspace/bitstream/2013/149964/1/Power-aware2008.pdf

20. Vander Biest, A., Richard, A., **Milojevic, D.**, & Robert, F. (2007). A framework introducing model reversibility in SoC design space exploration. *Lecture notes in computer science*, *4599 LNCS*, 211-221.

21. **Milojevic, D.**, & Van Ham, P. (2005). Bit-serial implementation of ranking filters on FPGAs. *Belgian journal of electronics and communication*, *1*, 11-13.

22. Colon, E., Hong, P., Habumuremyi, J.-C., Doroftei, I., Baudoin, Y., Shali, H., **Milojevic, D.**, & Weemaels, J. (2002). An integrated robotic system for antipersonnel mines detection. *Control engineering practice*, *10*(11), 1283-1291.

23. Schachne, M. M., van Kempen, L., **Milojevic, D.**, Sahli, H., Van Ham, P., Acheroy, M., & Cornelis, J. (1998). Mine detection by means of dynamic thermography: Simulation and experiments. *IEE Conference Publication*,(458), 124-127.

24. Winand, R., Van Ham, P., Colin, R., & **Milojevic, D.** (1997, February). An attempt to quantify electrodeposit metallographic growth structures. *Journal of the Electrochemical Society*, *144*(2), 428-436.

4. Articles published in conference proceedings

1. Luca, M., Gerousis, V., & **Milojevic, D.** (2018). Efficient place and route enablement of 5-tracks standard- cells through EUV compatible N5 ruleset. *SPIE*.

2. Luca, M., Debacker, P., & **Milojevic, D.** (2017). IR-drop aware Design & Technology Co-Optimization for N5 node with different device and cell height options. *ICCAD Conference*.

3. Allard, Y., **Milojevic, D.**, & Goossens, J. (2017). Can we get a predictable cache system for real-time computer systems? *Heterogeneous Architectures and Real-Time Systems*.

4. **Milojevic, D.** (2017). Library-level characterization of sub-10nm processing nodes. *CDNLive EMEA*.

5. Palomar, O., Rethinagiri, S., Yalcin, G., Titos-Gil, R., Prieto, P., Torrella, E., Unsal, O., Cristal, A., Felber, P., Sobe, A., Hayduk, Y., Kurpicz, M., Fetzer, C., Knauth, T., Schneegass, M., Struckmeier, J., & **Milojevic, D.** (2016). The ParaDIME project. *Design Automation and Test in Europe (DATE2016)*.

6. Yalcin, G., Rethinagiri, S. K., Palomar, O., Unsal, O., Cristal, A., & **Milojevic, D.** (2016). Exploring Energy Reduction in n10 Future Nodes via Voltage Scaling. *24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP 2016)*.

7. Palomar, O., Rethinagiri, S., Yalcin, G., Titos-Gil, R., Prieto, P., Torrella, E., Unsal, O., Cristal, A., Felber, P., Sobe, A., Hayduk, Y., Kurpicz, M., Fetzer, C., Knauth, T., Schneegass, M., Struckmeier, J., & **Milojevic, D.** (2016). Energy Minimization at All Layers of the Data Center: The ParaDIME Project. *Proceedings of the 2016 Conference on Design, Automation AND Test in Europe* (pp. 684-689). EDA Consortium. (DATE '16).

8. Yalcin, G., Rethinagiri, S., Palomar, O., Unsal, O., Cristal, A., & **Milojevic, D.** (2016). Exploring Energy Reduction in Future Technology Nodes via Voltage Scaling with Application to 10nm. *2016 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP)* (pp. 184-191). doi:10.1109/PDP.2016.108

9. Ku, B. W., Debacker, P., **Milojevic, D.**, Raghavan, P., & Lim, S. K. (2016). How Much Cost Reduction Justifies the Adoption of Monolithic 3D ICs at 7Nm Node? *Proceedings of the 35th International Conference on Computer-Aided Design* (pp. 87:1-87:7). ACM. (ICCAD '16). doi:10.1145/2966986.2967044

10. Ku, B. W., Debacker, P., **Milojevic, D.**, Raghavan, P., Verkest, D., Thean, A., & Lim, S. K. (2016). Physical Design Solutions to Tackle FEOL/BEOL Degradation in Gate-level Monolithic 3D ICs. *Proceedings of the 2016 International Symposium on Low Power Electronics and Design* (pp. 76-81). ACM. (ISLPED '16). doi:10.1145/2934583.2934622

11. Beece, A., **Milojevic, D.**, Plas, G. V. D., Augur, R., Sureddin, M., Singh, J., Senapati, B., Bouche, G., Alapati, R., Stephens, J., Lin, I., Rashed, M., Yuan, L., Kye, J., Woo, Y., Wehbi, A., Hang, P., Ton-that, V., Kanagala, V., Yu, D., Gao, S., & Samavedam, S. (2015). Quantitative Projections of the Cost Benefits of 3D Integration. *International Microelectronics Assembly and Packaging Society (IMAPS) 48th Conference*.

12. **Milojevic, D.** (2015). Advanced integration technologies: heterogeneous system design opportunities and challenges. *Programmability: Programming Models for Large Scale Heterogeneous Systems, HIPEAC*.

13. **Milojevic, D.** (2015). 3D-Stacked Integrated Circuits: From technology to application. *ARCHI2015*.

14. Maggioni, F. L. T., Oprins, H., **Milojevic, D.**, Beyne, E., Wolf, I. D., & Baelmans, M. (2015). 3D-Convolution Based Fast Transient Thermal Model for 3D Integrated Circuits: Methodology and Applications. *Thermal Measurement, Modeling Management Symposium (SEMI-THERM), 2015 31st,* (pp. 107-112). doi:10.1109/SEMI-THERM.2015.7100148

15. Agrawal, P., **Milojevic, D.**, Raghavan, P., Catthoor, F., Van der Perre, L., Beyne, E., & Varadarajan, R. (2014). 2D vs 3D integration: Architecture-technology co-design for future mobile MPSoC platforms. *Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), 2014 IEEE International* (pp. 381-384). doi:10.1109/IITC.2014.6831839

16. Allard, Y., Nelissen, G., Goossens, J., & **Milojevic, D.** (2014). A context aware cache controller to bridge the gap between theory and practice in real-time systems. *Embedded and Real-Time Computing Systems and Applications (RTCSA), 2014 IEEE 20th International Conference on* (pp. 1-10). doi:10.1109/RTCSA.2014.6910503

17. **Milojevic, D.**, Marchal, P., Marinissen, E. J., Plas, G. V. D., Verkest, D. D., & Beyne, E. (2013). Design Issues in Heterogeneous 3D/2.5D Integration. *ASP-DAC*.

18. **Milojevic, D.** (2013). Will 3D-IC Remain a Technology of the Futureldots Even in the Future? *DATE 2013*.

19. Casale-Rossi, M., Leduc, P., De Micheli, G., Blouet, P., Farley, B., Fontanelli, A., **Milojevic, D.**, & Smith, S. G. (2013). Will 3D-IC remain a technology of the future; Even in the future? *Design, Automation Test in Europe Conference Exhibition (DATE), 2013* (pp. 1526-1530). doi:10.7873/DATE.2013.310

20. **Milojevic, D.**, Idgunji, S., Jevdjic, D., Ozer, E., Lotfi-Kamran, P., Panteli, A., Prodromou, A., Nicopoulos, C., Hardy, D., Falsafi, B., & Sazeides., Y. (2012). Thermal Characterization of Cloud Workloads on a Power-Efficient Server-on-Chip. *30th Intl. IEEE Conference on Computer Design (ICCD)*.

21. **Milojevic, D.**, Marinissen, E. J., & Plas, G. V. D. (2012). Industry collaboration in 3-D IC tools. *EE-Times --- Are 3D ICs ready for Prime Time?*.

22. **Milojevic, D.**, & Varadarajan, R. (2012). SpyGlass Physical 3D. *DAC2012*.

23. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2012). An Efficient Algorithm Optimizing the Number of Processors to Schedule Multi-Threaded Tasks. *in submission at RTAS 2012*.

24. Eneman, G., Cho, J., Moroz, V., **Milojevic, D.**, Choi, M., De Meyer, K., Mercha, A., Beyne, E., Hoffmann, T., & Van der Plas, G. (2011). An Analytical Compact Model for Estimation of Stress in Multiple Through-Silicon Via Configurations. *Design, Automation & Test in Europe*.

25. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2011). Optimizing the Number of Processors to Schedule Multi-Threaded Tasks. *In Proceedings of the 32nd IEEE Real-Time Systems Symposium (Work in Progress session - RTSS11-WiP)*.

26. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2011). Reducing Preemptions and Migrations in Real-Time Multiprocessor Scheduling Algorithms by Releasing the Fairness. *RTCSA (1)* (pp. 15-24).

27. Nelissen, G., Funk, S., Goossens, J., & **Milojevic, D.** (2011). Swapping to Reduce Preemptions and Migrations in EKG. *23rd Euromicro Conference on Real-Time Systems (Work in Progress session)*.

28. Allard, Y., Goossens, J., & **Milojevic, D.** (2011). Creating a debugging environment to validate real-time scheduling algorithms. *SNUG*. Synopsys.
https://dipot.ulb.ac.be/dspace/bitstream/2013/151598/1/snug_2011_article.pdf

29. Doan, N. A. V., Robert, F., De Smet, Y., & **Milojevic, D.** (2010, September). MCDA-based methodology for efficient 3d-design space exploration and decision. *International Symposium on System-on-Chip Proceedings* (pp. 76-83).

30. Nelissen, G., Berten, V., Goossens, J., & **Milojevic, D.** (2010). An Optimal Multiprocessor Scheduling Algorithm without Fairness. *Proceedings of the 31th IEEE Real-Time Systems Symposium (Work in Progress session - RTSS10-WiP)*.
https://dipot.ulb.ac.be/dspace/bitstream/2013/71331/1/71331.pdf

31. Richard, A., **Milojevic, D.**, Robert, F., Bartzas, A., Papanikolaou, A., Siozios, K., & Soudris, D. (2010). Fast Design Space Exploration Environment Applied on NoC's for 3D-Stacked MPSoC's. *ARCS '10 - 23th International Conference on Architecture of Computing Systens 2010*.

32. Perry, D., Marchal, P., & **Milojevic, D.** (2010). Case study: Definition and Pathfinding of a GPU. *D43D: 2nd Design for 3D Silicon Integration Workshop*.

33. Doan, N. A. V., De Smet, Y., Robert, F., & **Milojevic, D.** (2010). On the use of multi-criteria decision aid tools for the efficient design of 3D-stacked integrated circuits: a preliminary study. *Industrial Engineering and Engineering Management Proceedings* (pp. 957-962). Macao.

34. Nelissen, G., Nélis, V., Goossens, J., & **Milojevic, D.** (2009). High-level simulation for enhanced context switching for real-time scheduling in MPSoCs. In C. Seidner (Ed.), *Junior Researcher Workshop on Real-Time Computing* (pp. 47-50).

35. **Milojevic, D.**, Carlson, T., Croes, K., Radojcic, R., Ragett, D., Seynhaeve, D., Van der Plas, G., & Marchal, P. (2009). Automated Pathfinding tool chain for 3D-stacked integrated circuits: Practical case study. *3D System Integration*.

36. **Milojevic, D.**, Radojcic, R., Carpenter, R., & Marchal, P. (2009). Pathfinding: a design methodology for fast exploration and optimisation of 3D-stacked integrated circuits. *System-on-Chip, 2009* (pp. 118-123).

37. **Milojevic, D.** (2009). 3D-Stacked Integrated Circuits: Design Consequences, Architectural Aspects, Design Methodologies and Tools. *ACES 2009*.

38. **Milojevic, D.** (2009). Design Methodologies and EDA Tools for 3D-Stacked Integrated Circuits. *PhD School MUSICS*.

39. **Milojevic, D.** (2009). A multi-objective and hierarchical exploration tool for SoC peformance estimation. *Proceedings of HiPEAC Reconfigurable Computing Workshop*.

40. **Milojevic, D.** (2009). 3-D Integration from System Design Perspective. *System-on-Chip, 2009*.

41. Richard, A., Vander Biest, A., Bartzas, A., Papanikolaou, A., Soudris, D., **Milojevic, D.**, & Robert, F. (2009). A multi-criteria estimation tool for system-on-chip. *Date'09 University Booth*.

42. Nelissen, G., Nélis, V., Goossens, J., & **Milojevic, D.** (2009). High-Level Simulation for Enhanced Context Switching for Real-Time Scheduling in MPSoCs. *Proceedings of the 3rd Junior Researcher Workshop on Real-Time Computing* (pp. 47-50).

43. Marchal, P., **Milojevic, D.**, Raghavan, P., & Verkest, D. D. (2008). PathFinding - Determining the technology/design sweetspot. *3D IC Design and Architecture Workshop*.

44. Leroy, A., Picalausa, J., **Milojevic, D.**, Robert, F., & Verkest, D. D. (2007). Quantitative Comparison of Switching Strategies for Networks on Chip. *Southern Conference on Programmable Logic (SPL) 2007*.

45. Engels, L., **Milojevic, D.**, & Warzée, N. (2007). 3D and Virtual Reality: Tools For Archaeological Hypothesis Verification. *Proceedings of IEEE VRIC 2007* (pp. 203-208).

46. Vander Biest, A., & **Milojevic, D.** (2007). Framework for fast performance evaluation of flexible models applied to interconnect delay. *Proceedings of the workshop on Design and Architectures for Signal and Image Processing*.

47. **Milojevic, D.**, Verkest, D. D., & Montperrus, L. L. (2007). Power dissipation of the Network-on-Chip in a System-on-Chip for MPEG-4 video encoding. *Solid-State Circuits Conference* (pp. 392-395).

48. Vander Biest, A., Leroy, A., **Milojevic, D.**, & Robert, F. (2006). A flexible system-level design methodolofy applied to NoC. *Special Inaugural Workshop on Future Interconnects and Networks on Chip, DATE (Design Automation and Test in Europe Conference) 2006*.

49. Vander Biest, A., **Milojevic, D.**, & Robert, F. (2006). Key enablers for next generation system-level design in microelectronics. *Proceedings of the 10th World Multi-Conference on Systemics, Cybernetics and Informatics*.

50. Helin, G., **Milojevic, D.**, & Warzée, G. (2005). Hierarchical modeling: virtual tour of the crypt in Brussels cathedral. *Proceedings of Virtual Retrospect 2005* (pp. 602-605).

51. Helin, G., **Milojevic, D.**, & Warzée, N. (2005). Modélisation hiérarchique: visite virtuelle de la crypte de la cathédrale de Bruxelles. *Pre-Proceedings of Virtual Retrospect 2005* (pp. 71-75).

52. **Milojevic, D.**, Laugerotte, C., Dunham, P., & Warzée, N. (2005). Computers and 3D Image Synthesis as Tools for Archaeology. *Computer as a Tool, 2005. EUROCON 2005.The International Conference on* (pp. 1036-1039).

53. Helin, G., **Milojevic, D.**, & Warzée, N. (2005). Hierarchical Modeling: Virtual Visit of the Bruxelles Cathedral. *Virtual retrospect conference 2005* (pp. 602-605).

54. **Milojevic, D.** (2005). Implementation of Ranking Filters on General Purpose and Reconfigurable Architecture Based on High Density FPGA Devices. *Field Programmable Logic and Applications, 2005. International Conference on* (pp. 602-605).

55. Debeir, O., **Milojevic, D.**, Leloup, T., Van Ham, P., Kiss, R., & Decaestecker, C. (2005). Mitotic Tree Construction by Computer In Vitro Cell Tracking : a Tool for Proliferation and Motility Features Extraction. *Proc. of the EUROCON 2005* (pp. 951-954). IEEE, Piscataway.
https://dipot.ulb.ac.be/dspace/bitstream/2013/53176/1/Eurocon2005_celltracking.pdf

56. **Milojevic, D.** (1999). Mathematical morphology and Parallel reconfigurable systems based on FPGAs. *International Symposium on Pattern Recognition In Memoriam Pierre Devijver*.

57. **Milojevic, D.** (1999). Fast computation of the mean value using parallel reconfigurable systems based on FPGAs. *International Symposium on Humanitarian Demining: HUDEM*.

58. **Milojevic, D.**, Colon, E., Hong, P., & Doroftei, I. (1999). A versatile scanner for systematic acquisition of multisensor data. *Photomec99 - European workshop*.

59. Schachne, M. M., van Kempen, L., **Milojevic, D.**, Sahli, H., Van Ham, P., & Cornelis, J. (1998). Mine detection by means of dynamic thermography: simulation and experiments. *Proceedings of the Second International Conference on The Detection of Abandoned Land Mines*.

60. **Milojevic, D.**, & Van Ham, P. (1996). Morphologie mathématique et architectures parallèles. *Actes de la 19e Journée de l'ISS France*.

5. Oral presentations during conferences, which include a review committee

1. **Milojevic, D.** (2016). *3D Technology Driven by 3D Application Requirements*. Paper session presented at DATE, Hot Topic3.2: 3D ICs: Leap Forward to 1,000X Performance (Dresden, Germany).

2. **Milojevic, D.** (2009). *PathFinding - Design Methodology for 3D-Stacked Integrated Circuits: Tool Chain and Case Studies*. Paper session presented at Seminar (National University of Athens, Athens, Greece).

3. Vander Biest, A., Richard, A., **Milojevic, D.**, & Robert, F. (2007). *Développement et validation d'outils de CAO électronique/microélectronique implémentant une méthodologie de co2design*. Paper session presented at Ecole d'hiver Francophone sur les Technologies de Conception des systèmes embarqués Hétérogènes (10-12 January 2007: Villard-de-Lans, France).